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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	DB3
First Inventor or Application Identifier	BRADDOCK
Title	INTEGRATED TRANSISTOR DEVICES
Express Mail Label No.	EL193169256US

JC882 U.S. PTO 09/636484 08/10/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 13] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

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5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [ ] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [X] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
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STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONCERN

Docket Number (Optional): DB3

Applicant, Patentee, or Identifier: BRADDOCK
Application or Patent No.: 60/201,739 PROVISIONAL DATED 4 MAY 2000
Filed or Issued: 5-4-2000
Title: INTEGRATED TRANSISTOR DEVICES

I hereby state that I am
☒ the owner of the small business concern identified below:
☐ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN: OSEMI, INC.

ADDRESS OF SMALL BUSINESS CONCERN: 300 FIRST ST NE
ROCHESTER, MN 55906

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☒ the specification filed herewith with title as listed above.
☒ the application identified above.
☒ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

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☐ no such person, concern, or organization exists.
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I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

NAME OF PERSON SIGNING: WALTER DAVID BRADDOCK IV

TITLE OF PERSON IF OTHER THAN OWNER:

ADDRESS OF PERSON SIGNING: 1128 FIRST ST NW ROCHESTER, MN 55906

SIGNATURE: WALTER DAVID BRADDOCK DATE: 8-10-2000

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1 UTILITY PATENT APPLICATION TRANSMITTAL FORM

2 CHECK FOR $576.00 TO 'COMMISIONER OF PATENTS AND TRADEMARKS"

3 FEE TRANSMITTAL FORM FOR FY 2000

4 DECLARATION

5 STATEMENT OF SMALL ENTITY STATUS—SMALL BUSINESS CONCERN

6 UTILITY PATENT INVENTION DISCLOSURE, 13 PAGES INCLUDING 2 FIGURES

INVENTOR: WALTER DAVID BRADDOCK
ENTITLED: INTEGRATED TRANSISTOR DEVICES
13 PAGES OF WRITTEN DESCRIPTION INCLUDING 2 FIGURES

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DAVID BRADDOCK
OSEMI INC
300 FIRST ST NE
ROCHESTER, MN 55906

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This application claims priority under 35.USC.119(e) to Provisional application #60/201,739 filed on 4 May 2000, listing Walter David Braddock as Inventor

Integrated Transistor Devices

Abstract

A self-aligned enhancement mode metal-oxide-compound semiconductor field effect transistor (10) includes a lower oxide layer that is a mixture of Ga_2O, Ga_2O_3, and other gallium oxide compounds (30), and a second insulating layer that is positioned immediately on top of the gallium oxygen layer.together positioned on upper surface (14) of a III-V compound semiconductor wafer structure (13). Together the lower gallium oxide compound layer and the second insulating layer form a gallium oxide gate insulating structure. The gallium oxide gate insulating structure and underlying compound semiconductor gallium arsenide layer (15) meet at an atomically abrupt interface at the surface of with the compound semiconductor wafer structure (14). The initial essentially gallium oxygen layer serves to passivate and protect the underlying compound semiconductor surface from the second insulating oxide layer. A refractory metal gate electrode layer (17) is positioned on upper surface (18) of the second insulating oxide layer. The refractory metal is stable on the second insulating oxide layer at elevated temperature. Self-aligned source and drain areas, and source and drain contacts (19, 20) are positioned on the source and drain areas (21, 22) of the device. Multiple devices are then positioned in proximity and the appropriate interconnection metal layers and insulators are utilized in concert with other passive circuit elements to form a integrated circuit structure.

Inventors: **Braddock, Walter David** (Rochester MN)
Assignee: **OSemi Inc.** (Rochester, MN)

Appl. No.:
Filed: **August 9, 2000**

U.S. Class:	**257/410**; 257/192; 257/631
Intern'l Class:	H07L 029/78
Field of Search:	257/410,411,192,631

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Primary Examiner:
Attorney, Agent or Firm:

Figures

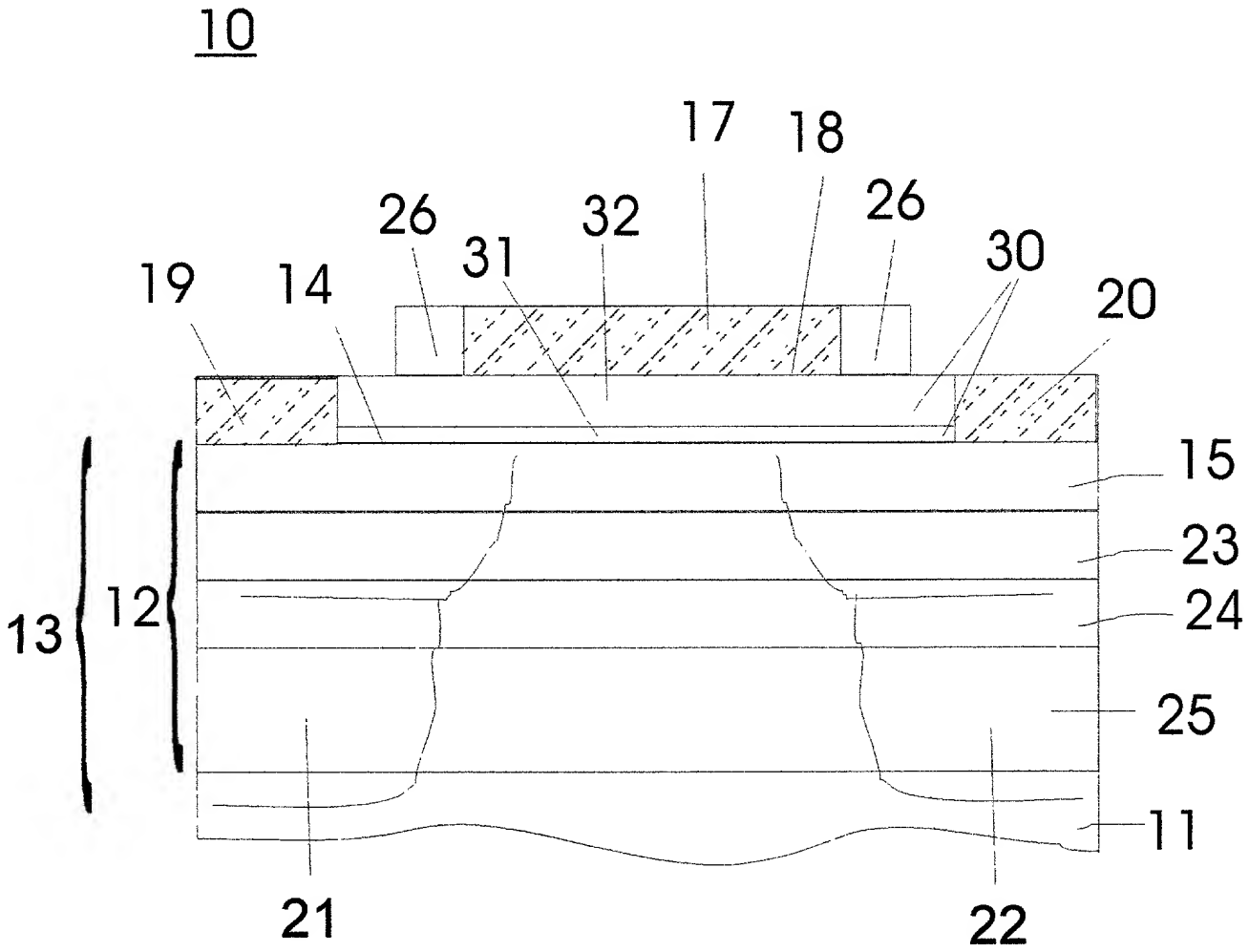

Figure 1

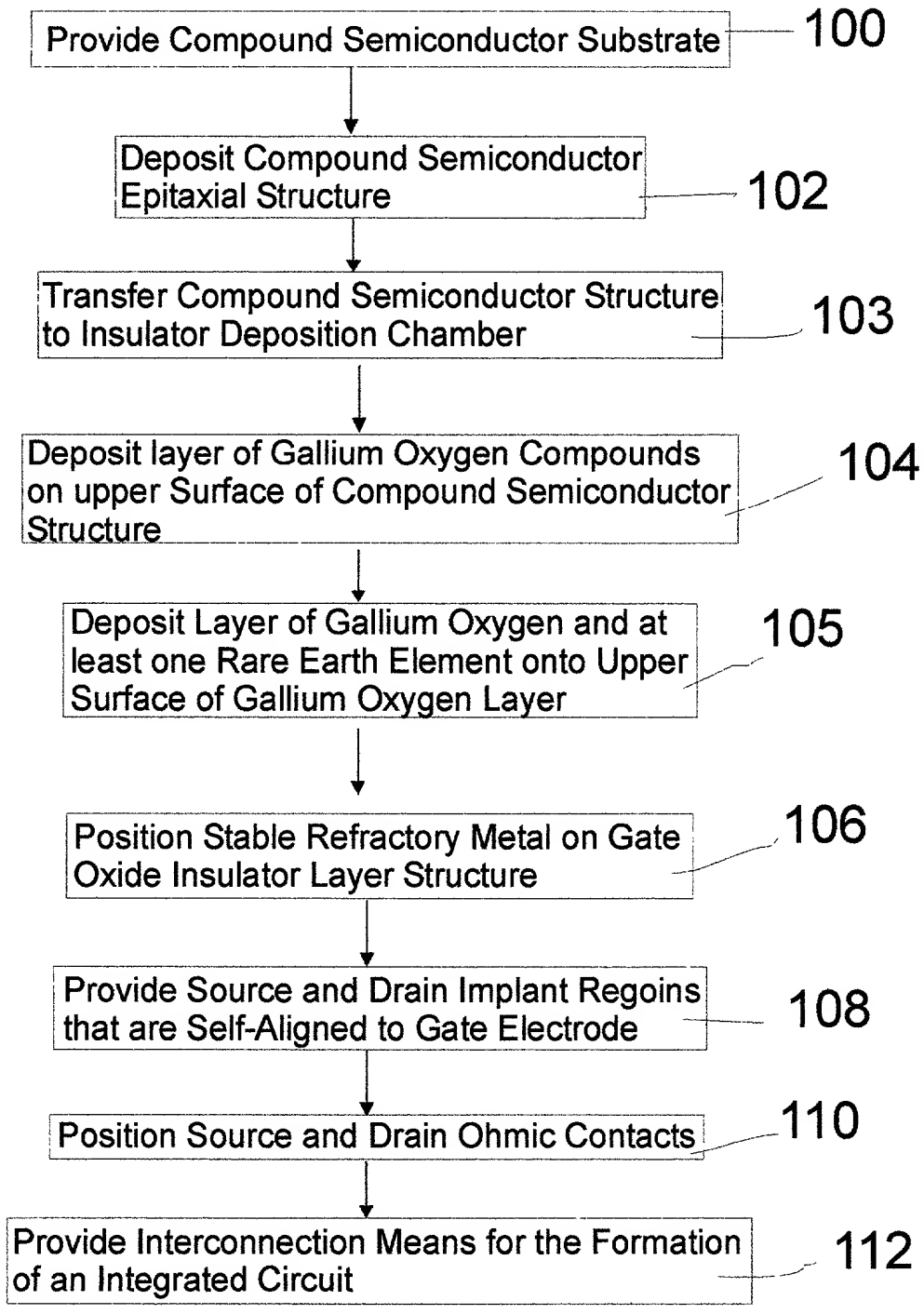
Provide Compound Semiconductor Substrate
100
Deposit Compound Semiconductor Epitaxial Structure
102
Transfer Compound Semiconductor Structure to Insulator Deposition Chamber
103
Deposit layer of Gallium Oxygen Compounds on upper Surface of Compound Semiconductor Structure
104
Deposit Layer of Gallium Oxygen and at least one Rare Earth Element onto Upper Surface of Gallium Oxygen Layer
105
Position Stable Refractory Metal on Gate Oxide Insulator Layer Structure
106
Provide Source and Drain Implant Regoins that are Self-Aligned to Gate Electrode
108
Position Source and Drain Ohmic Contacts
110
Provide Interconnection Means for the Formation of an Integrated Circuit
112

Figure 2

Description

FIELD OF THE INVENTION

The present invention pertains to low power and high speed integrated circuits in the compound semiconductor field utilizing field effect transistors and more specifically complementary field effect transistors used in concert including enhancement mode self-aligned metal-oxide-compound semiconductor transistors and depletion mode self-aligned metal-oxide-compound semiconductor transistors and methods of materials growth and fabrication of said structures and the ultra large scale integration of said transistors.

BACKGROUND OF THE INVENTION

The gallium arsenide and indium phosphide integrated circuit industry has been limited without a technology that simultaneously allows the integration of complementary field effect transistor devices and transistors with low gate leakage currents. In contrast to silicon technology that has a very mature and useful complementary metal oxide semiconductor (CMOS) technology. Field effect transistor (FETs) widely used in the III-V semiconductor industry employ metal gates and Schottky gate contacts that are have quiescent-state leakage currents exceeding many microamps. The use of metal gates in compound semiconductor technology further results in individual transistors and integrated circuits that have excessively high power dissipation, reduced transconductance, reduced logic swing and the inability to operate on a single power supply, and generally limited performance characteristics. The high magnitude of the quiescent leakage current limits the maximum integration of GaAs devices to circuits of several hundred thousand transistors for those skilled in the art. In contrast, the simultaneous integration of many millions of transistors is possible at high integration densities using silicon CMOS technology. These ultra high integration densities and levels cannot be obtained using metal, Schottky-style gates that are not insulated in compound semiconductor FETs. Thus Si CMOS technology offers significant advantages in terms of individual gate leakage, circuit integration level and cost.

However when compared to silicon, complementary GaAs and InP circuit technology exhibits faster and more optimized speed/power performance and efficiency at a low supply voltage of 1V and below. The market acceptance of these GaAs and InP integrated circuit technologies remains low because of the lack of ability to demonstrate high integration densities with low amounts of operating power. Thus, silicon CMOS dominates the field of digital integrated circuitry and neither GaAs nor InP technologies can successfully penetrate this market.

What is needed are new and improved compound semiconductor field effect transistors (FET). What is also needed are new and improved compound semiconductor FETs using metal-oxide-semiconductor junctions (MOSFET). What is also needed are new and improved compound semiconductor MOSFETs using a self-aligned gate structure. What is also needed are new and improved self-aligned compound semiconductor MOSFETs using enhancement mode and depletion mode operation. What is also needed are new and improved self-aligned compound semiconductor MOSFETs with stable and reliable device operation. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which enable optimum compound semiconductor device performance. What is also needed are new and improved self-aligned compound semiconductor MOSFETs with optimum efficiency and output power for RF and microwave applications. What is also needed are new and improved self-aligned compound semiconductor MOSFETs for use in complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs for low power/high performance complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which offer the design flexibility of complementary architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which keep interconnection delays in ultra large scale integration under control. What is needed are new and useful complementary integrated circuits where each individual transistor has a leakage current approaching 10^{-12} amp. What is needed is a truly useful integrated circuit technology for GaAs and InP that allows for the useful and economical operation of ULSI digital integrated circuits in compound semiconductors. What is needed are new and improved compound semiconductor MOSFET integrated circuits with very low net power dissapation. What is needed are new and improved compound semiconductor MOSFET devices with low gate leakage currents that may be integrated together to form ultra large

scale integrated circuits that include millions of transistors. What is needed are new and improved complementary MOSFET devices and circuits in compound semiconductors that allow the direct use, transfer and application of silicon CMOS design that already exits in the art.

What is also needed are new and improved methods of fabrication of self-aligned compound semiconductor MOSFETs. What is also needed is new and improved methods of fabrication of self-aligned compound semiconductor MOSFETs which are compatible with established complementary GaAs heterostructure FETs technologies. What is also needed are new and improved compound semiconductor MOSFETs which are relatively easy to fabricate and use.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the figures, wherein like reference numbers refer to similar items throughout the figures, and:

FIG. 1 is simplified cross sectional view of a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention;

FIG. 2 is a simplified flow chart illustrating a method of manufacturing a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention.

The exemplification set out herein illustrates a preferred embodiment of the invention in one form thereof, and such exemplification is not intended to be construed as limiting in any manner.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention provides, among other things, a self-aligned enhancement mode metal-oxide-compound semiconductor FET. The FET includes a gallium oxygen insulating structure that is composed of at least two distinct layers. The first layer is most preferably more that 10 angstroms thick but less that 25 angstroms in thickness and composed substantially of gallium oxygen compounds including but not limited to stoichiometric Ga_2O_3 and Ga_2O, and possibly a lesser fraction of other gallium oxygen compounds. The upper insulating layer in the gallium oxide insulating structure is composed of an insulator that does not intermix with the underlying gallium oxygen insulating structure. This upper layer must possess excellent insulating qualities, and is most typically composed of gallium oxygen and a third rare earth element that together form a ternary insulating material. Therefore the entire gallium oxide rare earth gate insulator structure is composed of at least two layers and may contain a third intermediate graded layers that consists of a mixture of the upper insulating material and the gallium oxygen compounds that compose the initial layer. Together the initial gallium oxygen layer, any intermediate graded layer and the top insulating region form both a gallium oxide insulating structure and the gate insulator region of a metal-oxide-compound semiconductor field effect transistor. The initial substantially gallium oxygen layer forms an atomically abrupt interface with the top layer of the compound semiconductor wafer structure, and does not introduce midgap surface states into the compound semiconductor material. A refractory metal gate electrode is preferably positioned on the upper surface of the gate insulator structure layer. The refractory metal is stable on the gate insulator structure layer at elevated temperature. Self-aligned source and drain areas, and source and drain contacts are positioned on the source and drain areas. In all embodiments preferred and otherwise, the metal-oxide-compound semiconductor transistor includes multi-layer gate insulator structure including an initial gallium oxygen layer, intermediate transition layer, and upper insulating layer of 30-250 angstroms in thickness positioned on upper surface of a compound semiconductor heterostructure that form the gate insulator structure. The preferred embodiment also comprises a compound semiconductor heterostructure including a GaAs, $Al_x Ga_{1-x}As$ and $In_y Ga_{1-y}As$ layers with or wothout n-type and/or p-type charge supplying layers which are grown on a compound semiconductor substrate, a refractory metal gate of W, WN, or WSi, self aligned donor (n-channel FET) or acceptor (p-channel FET) implants, and source and drain ohmic contacts. In another preferred embodiment, the compound semiconductor heterostructure comprises an $In_yGa_{1-y}As$, $Al_xIn_{1-x}As$, and InP compound semiconductor heterostructure and n-type and/or p-type charge supplying layers which are grown on an InP substrate, and a refractory metal gate of W, WN,

or WSi, self aligned donor (n-channel FET) or acceptor (p-channel FET) implants, and source and drain ohmic contacts.

FIG. 1 is simplified cross sectional view of a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention. Device 10 includes a compound semiconductor material, such as any III-V material employed in any semiconductor device, represented herein by a III-V semiconductor substrate 11 and a compound semiconductor epitaxial layer structure 12. For the purpose of this disclosure, the substrate 11 and any epitaxial layer structure 12 formed thereon will be referred to simply as a compound semiconductor wafer structure which in FIG. 1 is designated 13. Methods of fabricating semiconductor wafer structure 13 include, but are not limited to, molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD). It will of course be understood that in some specific applications, there may be no epitaxial layers present and upper surface of top layer 15 may simply be the upper surface of substrate 11.

Device 10 further comprises a gate insulator structures (30) that includes at least two or more layers. The first layer of the gate insulator structure (31) is composed entirely of gallium oxide compounds and is directly adjacent to and deposited upon the compound semiconductor structure. The second layer of the gate insulator structure (32) is composed of a compound of gallium, oxygen, and one or more rare earth elements from the periodic table. The initial gallium oxygen layer (31) forms an atomically abrupt interface 14 with the upper surface of top layer 15, the top layer of the compound semiconductor structure. A refractory metal gate electrode 17 which is stable in the presence of top insulating material at elevated temperature is positioned on upper surface 18 of the gate insulator structure. Dielectric spacers 26 are positioned to cover the sidewalls of metal gate electrode 17. Source and drain contacts 19 and 20 are deposited on self-aligned source and drain areas 21 and 22, respectively.

In a specific embodiment, the compound semiconductor epitaxial layer structure consists of a <11 angstrom GaAs top layer (15), a <101 angstrom $Al_xGa_{1-x}As$ spacer layer (23), a <251 angstrom $In_yGa_{1-y}As$ channel layer (24), and a GaAs buffer layer (25) grown on a GaAs substrate (11). Top GaAs layer (15) is used to form an atomically abrupt layer with the gate insulator structure with an abrupt interface with low defect density.

As a simplified example of fabricating a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention, a III-V compound semiconductor wafer structure 13 with an atomically ordered and chemically clean upper surface of top layer 15 is prepared in an ultra-high vacuum semiconductor growth chamber and transferred via a ultra high vacuum transfer chamber to a second ultra high vacuum oxide and insulator deposition chamber. The initial gallium oxygen layer (31) is deposited on upper compound semiconductor surface layer 15 using thermal evaporation from a high purity Ga_2O_3 source or from crystalline gadolinium gallium garnet, $Ga_3Gd_5O_{12}$. This initial gallium oxygen layer is deposited while holding the substrate temperature of the compound semiconductor structure at <580°C, and most preferably at a substrate temperature <495°C. After the deposition of approximately 18 angstroms of gallium oxygen compounds in the insulator deposition chamber over a 5 to 8 minute period of time, deposition of the second insulator layer is initiated. The deposition of the second insulator layer starts by directing the flux from a low power oxygen plasma source into the ultra high vacuum system such that the oxygen plasma effluent and species are largely directed toward and impinging upon said compound semiconductor structure with initial gallium oxygen layer. The flux from the oxygen plasma source should be directed at the surface for between 2-5 seconds, subsequently followed by the co-evaporation of gallium oxygen compounds from Ga_2O_3 and a second thermal evaporation source that contains a rare-earth element. The flux beams from the oxygen source, Ga_2O_3 and rare-earth evaporation source thermal evaporation sources are carefully balanced to provide a ternary insulator layer on top of the initial gallium oxygen layer on said compound semiconductor structure. As the deposition of the second ternary insulator layer is initiated, the substrate temperature is simultaneously adjusted to provide an optimized substrate temperature for the deposition of this layer. In this example the substrate temperature required to deposit the gallium+oxygen+rare earth layer is <530°C. The deposition of this second insulator layer proceeds until the total insulator thickness of 200-250 angstroms is achieved. Shutters and valves are utilized to stop the deposition of the ternary gallium+oxygen+rare earth layer upon the deposition of the required thickness of the insulator layer. The substrate temperature is cooled in-vacuum to approximately 200°C, and the deposition of a refractory metal which is stable and does not interdiffuse with on the top layer of the gate insulator structure at elevated temperature such as WSi or WN is deposited on upper surface 18 of oxide layer 32 and subsequently patterned using standard lithography. The refractory metal layer is

etched until oxide layer 31 is exposed using a refractory metal etching technique such as a fluorine based dry etching process. The refractory metal etching procedure does not etch the oxide layer 31, thus, oxide layer 31 functions as an etch stop layer such that upper surface of top layer 15 remains protected by oxide layer 31. All processing steps are performed using low damage plasma processing. Self-aligned source and drain areas 21 and 22, respectively are realized by ion implantation of Si (n-channel device) and Be/F or C/F (p-channel device) using the refractory metal gate electrode 17 and the dielectric spacers 26 as implantation masks. Such ion implantation schemes are compatible with standard processing of complementary compound semiconductor heterostructure FET technologies and are well known to those skilled in the art. The implants are activated at 700-900°C using rapid thermal annealing in an ultra high vacuum environment such that degradation of the interface 16 established between top layer 15 and oxide layer 31 is completely excluded. Finally, ohmic source and drain contacts 19 and 20 are deposited on the self-aligned source and drain areas 21 and 22, respectively. The devices may then be interconnected using the standard methods to those skilled in the art of integrated microelectronics and integrated circuit manufacture.

FIG. 2 is a simplified flow chart illustrating a method of manufacturing a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention. In step 102, a compound semiconductor wafer structure is produced using standard epitaxial growth methods in the art. In step 103, a layer consisting of gallium oxygen compounds including but not limited to Ga_2O_3 and Ga_2O is deposited on upper surface of said compound semiconductor wafer structure. In step 104, an insulating layer of gallium oxygen and one or more rare earth elements is deposited on the upper surface of the initial gallium oxygen compound layer. The gallium oxide gate insulator structure is formed in steps 104 and 105. In step 106, a stable refractory gate metal is positioned on upper surface of said gate insulator structure. In step 108, source and drain ion implants are provided self-aligned to the gate electrode. In step 110, source and drain ohmic contacts are positioned on ion implanted source and drain areas.

In a preferred embodiment, step 100 provides a compound semiconductor substrate such as GaAs or InP. Step 102 includes the preparation and epitaxial growth of an atomically ordered and chemically clean upper surface of the compound semiconductor wafer structure. Step 103 preferably comprises thermal evaporation from a purified and crystalline gadolinium gallium garnet or Ga_2O_3 source on an atomically ordered and chemically clean upper surface of the compound semiconductor wafer structure. Step 104 comprises the formation of a gallium+oxygen+rare earth elemental insulating layer formed through the simultaneous vacuum evaporation of gallium oxygen species and at least one rare earth element such as Gadolinium with the simultaneous oxidation using the effluent of an oxygen gas plasma source directed in simultaneous combination with other thermal evaporation sources toward substrate 100. The initial gallium oxygen compound layer of the gate insulator structure preferably functions as an etch stop layer such that the upper surface of the compound semiconductor wafer structure remains protected by the gate oxide during and after gate metal etching. The refractory gate metal desirably does not react with or diffuse into the gate oxide layer during high temperature annealing of the self-aligned source and drain ion implants. The quality of the interface formed by the gate oxide layer and the upper surface of the compound semiconductor structure is desirably preserved during high temperature annealing of the self-aligned source and drain ion implants. The self-aligned source and drain implants are desirably annealed at approximately 700°C in an ultra high vacuum environment. The self-aligned source and drain implants are desirably realized by positioning dielectric spacers on the sidewalls of the refractory gate metal.

Thus, new and improved compound semiconductor devices and methods of fabrication are disclosed. The new and improved self-aligned enhancement mode metal-oxide-compound semiconductor heterostructure field effect transistors enable stable and reliable device operation, provide optimum compound semiconductor device performance for low power/high performance complementary circuits and architectures, keep interconnection delay in ULSI under control, and provide optimum efficiency and output power for RF and microwave applications as well as for digital integrated circuits that require very high integration densities.

These improvements essentially solve or overcome the problems of the prior art, such as high gate leakage in compound semiconductor FET devices, low integration densities, dc electrical instability, and electrical hysterisis, and therefore provide a highly useful invention. While we have shown and described specific embodiments of the present invention, further modifications and improvements will occur to those skilled in the art. We desire it to be

understood, therefore, that this invention is not limited to the particular forms shown and we intend in the appended claims to cover all modifications that do not depart from the spirit and scope of this invention. What is claimed:

Claims

1. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a layer composed of the compounds of gallium and oxygen including but not limited to mixtures of Ga_2O_3, Ga_2O and other gallium oxygen compounds positioned on upper surface of said compound semiconductor wafer structure;

a second insulating layer composed of the compounds of gallium and oxygen and at least one or more rare earth elements that form an insulating layer deposited on top of the initial supporting gallium oxygen layer, with said first and second layers forming a gate insulator structure adjacent to and on top of the compound semiconductor structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layers;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein the refractory metal gate electrode comprises a refractory metal selected from the group consisting of W, WN or WSi or combinations thereof;

means of interconnection of said transistors forming a monolithically integrated circuit.

2. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial layer of gallium oxygen compounds forms an atomically abrupt interface with the upper surface of the compound semiconductor wafer structure.

3. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the gate insulator structure is composed of three layers, an initial gallium oxygen compound layer, a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element, and a third insulator layer that is composes largely of a compound of gallium, oxygen and one or more rare earth elements.

4. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the gate insulator structure is composed of more than three multiple layers, an initial gallium oxygen compound layer, and multiple layers containing gallium and oxygen with or without the inclusion of one or more rare earth elements that together form an insulating gallium oxide gate insulator structure.

5. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial gallium oxygen compound layer has a thickness of more than 10 angstroms and less than 25 angstroms.

6. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the gate insulator structure has an overall total thickness of 20-300 angstroms.

7. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial gallium oxygen compound layer forms an atomically abrupt interface with the compound semiconductor structure that extend less than four atomic layers in depth of structural interface modulation.

8. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial gallium and oxygen compound layer and the gate insulator structure protects the upper surface of the compound semiconductor wafer structure.

9. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the refractory metal gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at an elevated temperature of 700°C and above.

10. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the source and drain ion implants comprising said enhancement mode metal-oxide-compound semiconductor field effect transistor being an n-channel device or p-channel device.

11. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the source and drain ion implants comprise and Be/F or C/F, said enhancement mode metal-oxide-compound semiconductor field effect transistor being a p-channel device.

12. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the upper surface of the compound semiconductor wafer structure comprises GaAs.

13. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the upper surface of the compound semiconductor wafer structure comprises $In_xGa_{1-x}As$.

14. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a layer composed of the compounds of gallium and oxygen compounds including but not limited to mixtures of Ga_2O_3, Ga_2O and other gallium oxygen compounds positioned on upper surface of said compound semiconductor wafer structure;

a second insulating layer deposited upon the first composed of the compounds of gallium and oxygen and at least one or more rare earth elements such that the normalized relative composition of gallium, oxygen, and one or more rare earth elements are changing in a monotonic manner as a function of the thickness within said insulating layer;

a third insulating layer deposited on top of said second layer composed of gallium oxygen and at least one or more rare earth elements wherein said first, second and third layers form a gate insulator structure adjacent to and deposited on top of the compound semiconductor structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layers;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein the refractory metal gate electrode comprises a refractory metal selected from the group consisting of W, WN or WSi or combinations thereof;

means of interconnection of said transistors forming a monolithic integrated circuit.

15. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial layer of gallium oxygen compounds forms an atomically abrupt interface with the upper surface of the compound semiconductor wafer structure.

16. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the gate insulator structure is composed of three or more layers, an initial gallium oxygen compound layer, a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element, and a third insulator layer that is composes largely of a compound of gallium, oxygen and one or more rare earth elements.

17. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial gallium oxygen compound layer has a thickness of more than 10 angstroms and less than 25 angstroms.

18. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the gate insulator structure has an overall total thickness of 20-300 angstroms.

19. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial gallium oxygen compound layer forms an atomically abrupt interface with the compound semiconductor structure that extend less than four atomic layers in depth of modulation of said interface.

20. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial gallium and oxygen compound layer and the gate insulator structure protects the upper surface of the compound semiconductor wafer structure.

21. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the refractory metal gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at an elevated temperature of 700°C and above.

22. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the source and drain ion implants comprising said enhancement mode metal-oxide-compound semiconductor field effect transistor being an n-channel device.

23. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the source and drain ion implants comprise and Be/F and C/F, said enhancement mode metal-oxide-compound semiconductor field effect transistor being a p-channel device.

24. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the upper surface of the compound semiconductor wafer structure comprises GaAs.

25. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the upper surface of the compound semiconductor wafer structure comprises $In_xGa_{1-x}As$.

26. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure composed of alternating layers comprised of gallium, oxygen, at least one rare-earth element forming a gate insulator with low electronic midgap defect density positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein dielectric spacers are positioned on sidewalls of the stable refractory gate metal electrode.

27. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer.

28. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer is positioned between the gate oxide layer and the narrower band gap channel layer.

29. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer has a thickness of between 3-200 angstroms

30. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer comprises either $Al_xGa_{1-x}As$, InP, or $In_zGa_{1-z}P$ or a combination thereof.

31. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer has a thickness of 10-300 angstroms.

32. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer is positioned between the wider band gap spacer layer and a buffer layer.

33. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$.

34. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on upper surface of a compound semiconductor substrate.

35. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 34 wherein the compound semiconductor substrate includes a GaAs based semiconductor wafer.

36. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 34 wherein the compound semiconductor substrate includes a InP based semiconductor wafer.

37. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1, 13, 26, and 33 that may be integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuits.

* * * * *

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I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*
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Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] *OR* ☒ Correspondence address below

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
WALTER DAVID	BRADDOCK, IV

Inventor's Signature	WALTER DAVID BRADDOCK					**Date**	8-10-00
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☐ Additional inventors are being named on the ____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted with Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	DB3
First Named Inventor	WALTER DAVID BRADDOCK
COMPLETE IF KNOWN	
Application Number	60/201,739 — PROVISIONAL
Filing Date	5-4-2000
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

WALTER DAVID BRADDOCK, IV

(Title of the Invention)

the specification of which
☒ is attached hereto
OR
☐ was filed on (MM/DD/YYYY) ☐ as United States Application Number or PCT International Application Number ☐ and was amended on (MM/DD/YYYY) ☐ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
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☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	
60/201,739	05/04/2000	☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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